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OXIDE BARRIERS ON Ga As BY NEUTRAL ION BEAM SPUTTERING

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OXIDE BARRIERS ON GaAs BY NEUTRALIZED ION BEAM SPUTTERING*

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ABSTRACT

Tantalum and silicon oxides have been sputter deposited onto gallium arsenide using a 500 eV beam of neutralized argon atoms. MIS devices show very low leakage and capacitances that can be varied from full accumulation to depletion with the application of modest voltages. Other measurements (breakdown field, dielectric constant, adherence, Auger profile, and photoluminescence) also suggest that these structures hold potential usefulness for insulated gate GaAs circuitry.

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INTRODUCTION

The problem of preparing an insulating layer on gallium arsenide with properties suitable for a technologically viable MIS device has proven elusive. One important constraint on the fabrication of such devices is to keep the GaAs temperature below 750° to avoid formation of arsenic vacancies at the interface.[1] Thus, limitations are placed on both the fabrication temperature and any subsequent annealing cycles. Other constraints, if one can extrapolate from the more well understood Si-SiO_2 system, are that the chemical bonding must be strong and the impurity level low at the semiconductor-insulator interface.

Thermal oxides grown on GaAs have generally been too conductive to form an insulating barrier.[2] Anodically grown oxides[3] have good insulating properties, but have exhibited a substantial degree of charge trapping in the interfacial region. The microscopic nature of oxides grown in an aqueous environment and the effects of this environment have not yet been determined. Foster and Swartz[4] have grown silicon nitride layers by CVD which also had good insulating properties, but some charge trapping at the interface.

Plasma techniques for the growth and deposition of insulating layers on the III-V compounds provide interesting possibilities. Chang and Sinha[5] have recently demonstrated growth of an oxide on GaAs using an oxygen plasma. This oxide is somewhat conductive, but the interfacial properties look relatively good. Rf sputter deposition of Si_3N_4 on GaAs has been reported as far back as 1967.[6] The requirements of forming an insulating layer with high density and low interfacial charge seemed, however, to be

mutually incompatible with this technique. Quite possibly the interfacial charge results from the large amount of ion bombardment inherent to the diode rf sputtering system.

The present paper describes the application of a relatively new plasma technique for deposition of insulating layers. A beam of low energy argon ions is neutralized by passing it by a hot filament. The resulting plasma is used to sputter insulating materials without problems of charge buildup on either the target or the substrate.

FABRICATION PROCEDURE

The sputtering arrangement is shown schematically in Figure 1. The neutralized ion beam was produced by a 10 cm diameter Kaufman type source[7] supplied by Ion Tech, Inc. A bell jar pressure of $\sim 3 \times 10^{-4}$ torr argon was required to sustain the beam. Its energy can be varied from 100 to 800 eV/ion, and its current density from 0 to 2 ma/cm^2.

The gallium arsenide substrates used were Si doped wafers ($n = 1 \times 10^{18}$cm^{-3}) with either <100> or <111> orientation. These were mounted on a moveable platform to facilitate pre-deposition cleaning. In position A (Figure 1), the beam falls on the target, sputtering away the top layer, but these sputtered particles are shielded from the substrate. In position B, the substrate is cleaned using a reduced energy beam (100 eV, 0.2 ma/cm^2) for about five minutes, being mindful of possible sputter damage discussed below.

Actual sputtering takes place in position C. The angles and positions of the substrate and target are designed to give reasonably uniform coverage and still keep the substrate out of the beam path. Using 500 eV argon ions

with a density of 1 ma/cm^2, the deposition rates were approximately 40 Å/min for tantalum oxide sputtered from the metal, 10 Å/min when sputtered from Ta_2O_5 powder, and 30 Å/min for the silicon oxide sputtered from quartz. Final thickness ranged from 600 to 1800 Å. The substrate could be heated during deposition, but doing so generally produced inferior results.

As with other ion beam sputtered films,[8] we found the adherence and the abrasion resistance to be very good. Chemical etching and cleaning prior to the above steps made no observable difference to either the mechanical properties of the films or the electrical quality of the interface. Omission of the in situ ion beam etch, however, did yield films with poor adherence.

Part of the substrate is shielded from the ion beam to produce a step and facilitate interference thickness measurement. After the deposition is completed, several evaporated aluminum gates (0.8 mm diameter) are applied. Ohmic contact to the GaAs was achieved with alloyed Ni/Au-Ge films as described by Robinson.[9]

RESULTS

A summary of the results from the MIS structures produced is given in Table 1. These results can be described as typical of samples made after some time was spent optimizing procedures; changing thickness made no qualitative difference.

Preliminary to the primary measurements, we did some studies of the surface damage to the GaAs wafers during sputter cleaning. Wafers were etched with a solution of H_2SO_4:H_2O:H_2O_2(5:1:1) and with the ion beam.

No difference was observed in the carrier concentration or the mobility for the two processes. However, the Schottky barrier height using gold contacts, was reduced from 0.96 to 0.41 volts (using I-V and C-V measurements) when ion etching at 500 eV was substituted for the chemical etch. The depth of the damage was determined by timing how long a chemical etch was necessary to restore the barrier. This depth was less than 80 Å at 500 eV and presumably considerably less for the 100 eV bombardment actually used.

Photoluminescense spectra were taken to see if the ion etching produced trapping levels. No additional radiative transitions were observed. Auger profiles of the insulators on GaAs revealed no obvious impurities.

The current-voltage characteristic of the silicon oxide MIS structure from Column 3 of Table 1 is shown in Figure 2. The data do not give a good fit to either a Schottky diode or a bulk insulator trap conduction model. No significant difference was observed in the I-V curves from the two types of tantalum oxide targets, or the original silicon oxide fabrication. However, it was suspected that stray argon particles were sputtering the stainless steel fixturing and hence introducing metallic impurities in the oxide layers. Refixturing the apparatus using all quartz supports has, in fact, yielded silicon oxide layers with conductivities four orders of magnitude lower (see Table 1). Very recent results from silicon nitride have similarly shown very low conductivities.

Capacitance-voltage measurements were made at a frequency of 1 MHz using a Boonton model 72B capacitance meter. A plot for the tantalum structure is shown in Figure 3 and the comparable curve for the silicon

oxide structure (stainless steel fixturing) is depicted by Figure 4. The most salient feature is that the surface layer can be driven from full depletion to accumulation without dielectric breakdown.

All the C-V curves to date show the type of hysteresis suggestive of charge injection into the insulator.[10] The degree of hysteresis was somewhat lower with the silicon oxide. The minimum capacitances in Figures 3 and 4 suggest a substrate carrier concentration of $10^{17}cm^{-3}$, lower than the manufacturer's specification. Measurements on the lower conductivity silicon oxide layers, however, give a MIS capacitance minimum consistent with the GaAs carrier concentration.

DISCUSSION AND CONCLUSIONS

The devices reported here go into the deep depletion at large negative voltages. The evidence is that the minimum in capacitance is smaller than predicted from a calculation based on the known carrier concentration of the substrate material. The samples prepared in the improved deposition system have produced SiO_2 layers with resistivity of $10^{16}\Omega$-cm and the resulting MIS devices exhibited C-V characteristics consistent with the predictions of the calculation. It seems clear, therefore, that the conduction through the insulators was preventing the formation of an inversion layer at the surface of the GaAs. However, without quantitative information on the minority carrier lifetime for this sample, it is not possible to report exactly when the insulator conduction prevents inversion layer formation.

The surface state density for one of the Al-SiO_2-GaAs devices is shown in Figure 5. This calculation is based on the Terman method.[10] The

additional charge, ΔQ_{ss}, which is developed for the various band bending conditions, is found by measuring the voltage shift (ΔV) between the high-frequency capacitance and the ideal MIS capacitance. The charge is given by

$$\Delta Q_{ss} = C_{ox} \Delta V \quad ,$$

and the interface state density is given by

$$N_{ss} = \frac{1}{qA} \frac{d Q_{ss}}{d \psi_s} \quad ,$$

where ψ_s is the surface potential, q is the electronic charge, and A is the area of the capacitor plate.

The sputter deposited layers described here have been shown to have good insulating properties and have good adherence and physical properties. The surfaces of the n-type GaAs substrates used in the depositions have always been depleted after insulator deposition. It thus seems that the technique provides suitable electrically passivating layers on n-type GaAs. The charge trapping in the interfacial region of these insulators is still too large for them to be useful in constructing stable MIS devices. However, further refinement in the techniques should provide a definitive answer to their ultimate utility.

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TABLE 1. Summary of Data.

Target	Tantalum Oxide		Silicon Oxide	
	$Ta(O_2$ atm)	Ta_2O_5	SiO_2 (stainless fixturing)	SiO_2 (quartz fixturing)
Dielectric Constant	15-22	16-21	4.0	4.0
Resistivity [Ω-cm]	1×10^{12}	2×10^{11}	5×10^{10}	1×10^{16}
Flat Band Voltage	5	4	10	15
Surface Charge Concentration [cm^{-2}]	7×10^{12}	5×10^{12}	3×10^{12}	4×10^{12}
Breakdown Field [V/cm]	2×10^{6}	2×10^{6}	3×10^{6}	2×10^{6}

FIGURE CAPTIONS

Figure 1. Schematic of sputtering apparatus.

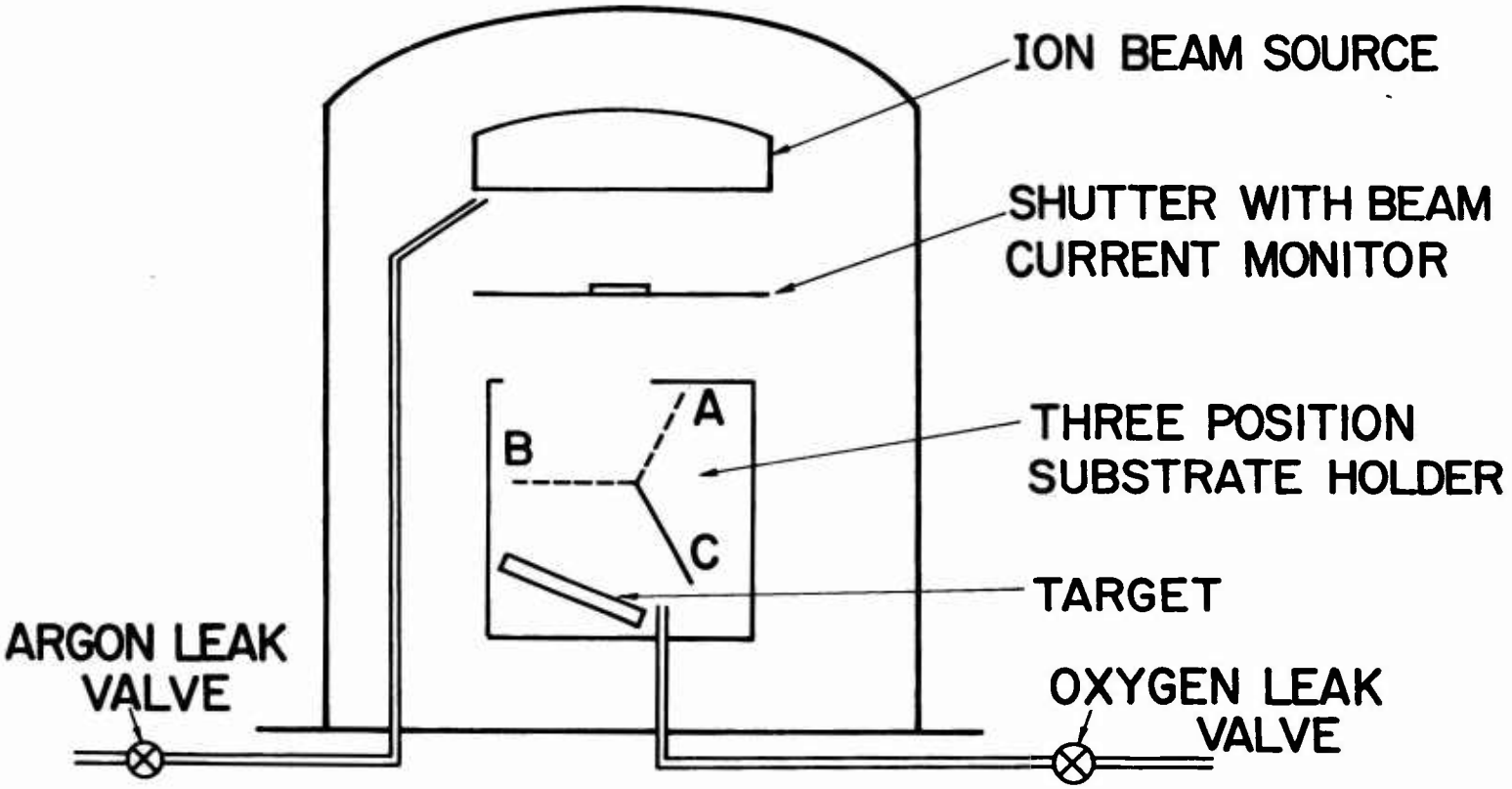
Figure 2. Current vs. voltage curve for 1000 Å silicon oxide film as fabricated using stainless steel fixturing.

Figure 3. Capacitance vs. voltage curve for Al-tantalum oxide-GaAs structure. Oxide thickness was 600 Å.

Figure 4. Capacitance vs. voltage curve for Al-silicon oxide-GaAs structure corresponding to Figure 2.

Figure 5. Surface state distribution for same silicon oxide sample.

FIG. 1


ION BEAM SOURCE
SHUTTER WITH BEAM CURRENT MONITOR
A
B
C
THREE POSITION SUBSTRATE HOLDER
TARGET
ARGON LEAK VALVE
OXYGEN LEAK VALVE

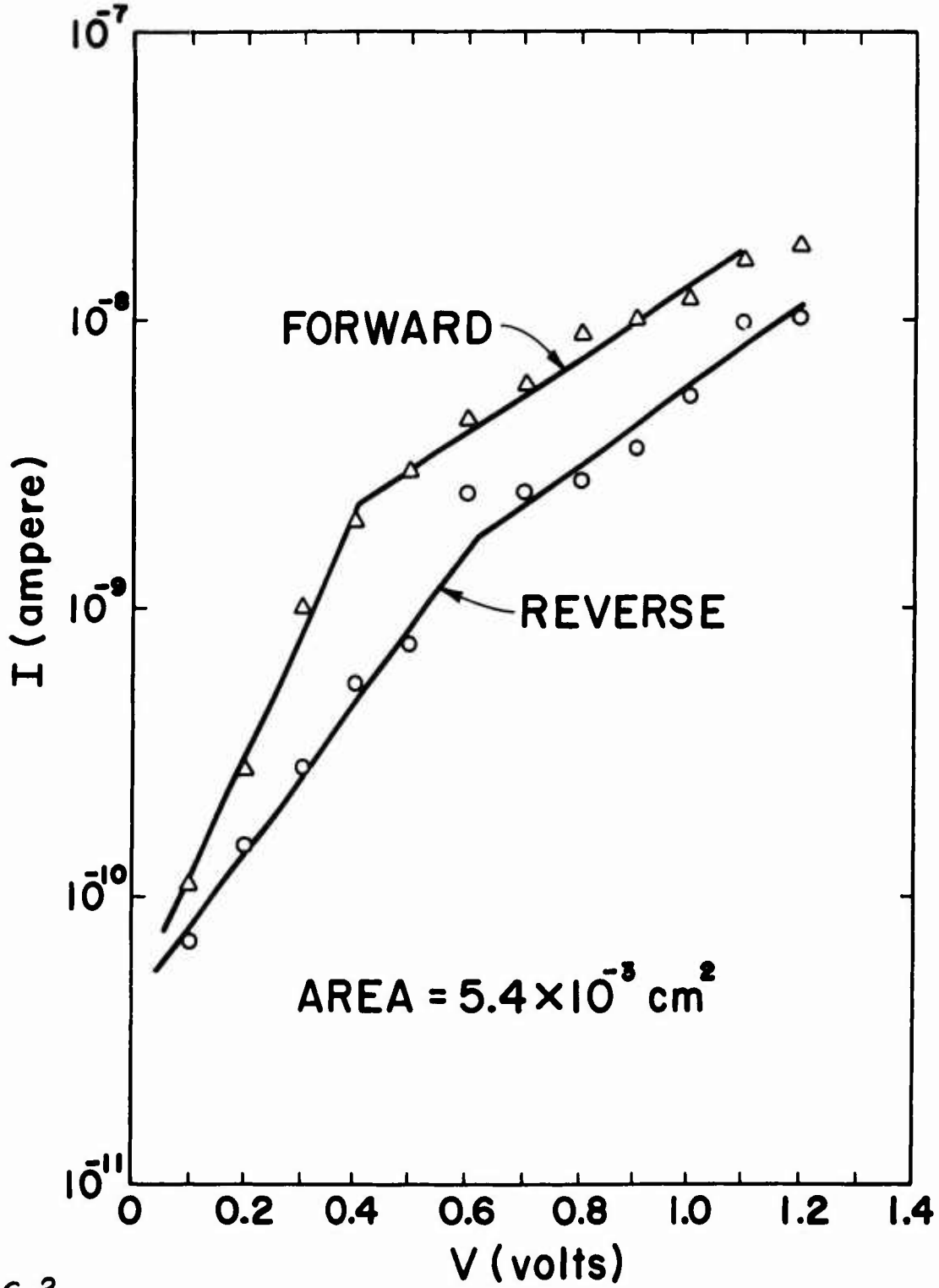

10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
I (ampere)
FORWARD
REVERSE
AREA = 5.4×10^{-3} cm^2
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
V (volts)

FIG. 2

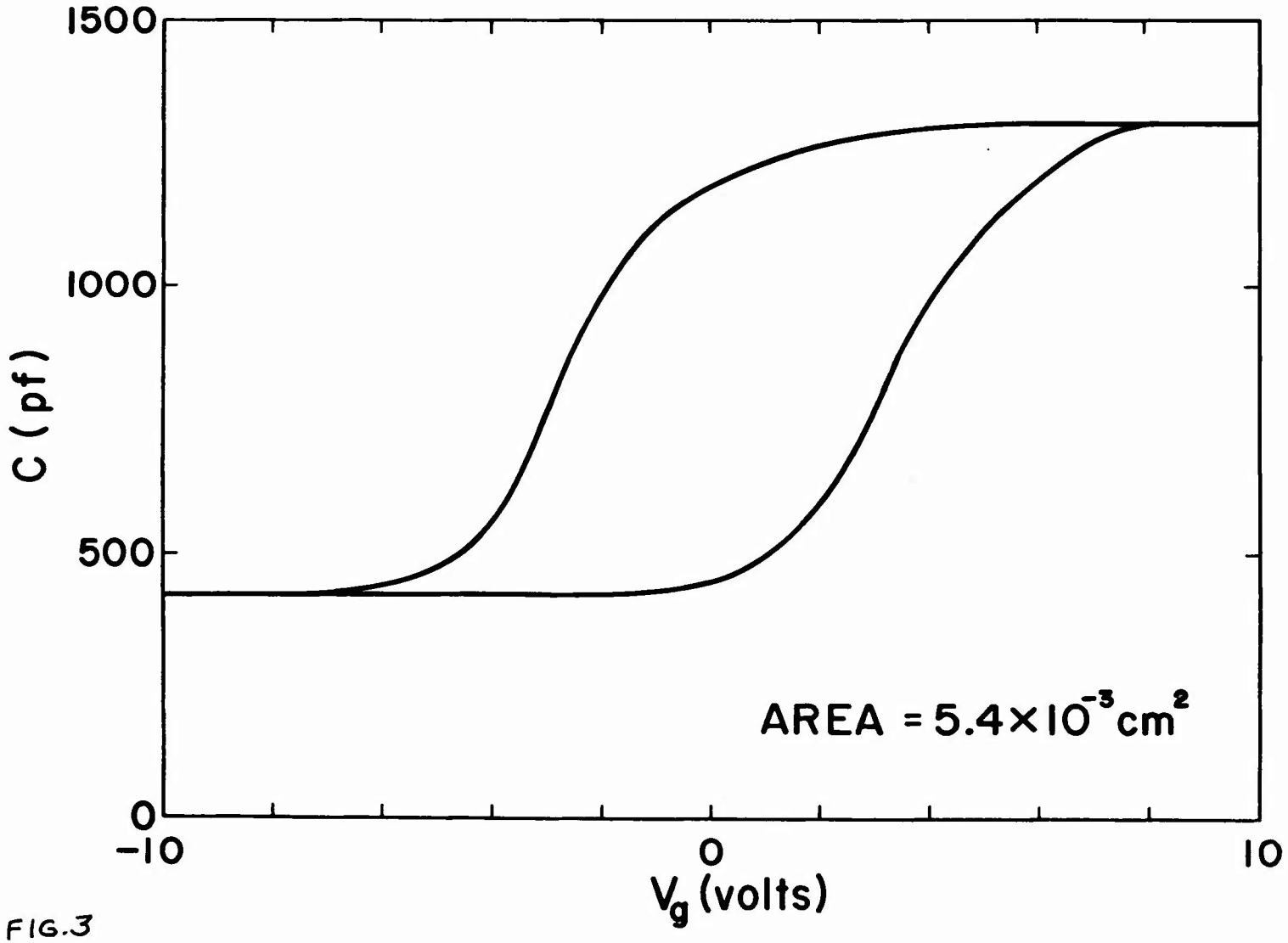


FIG.3

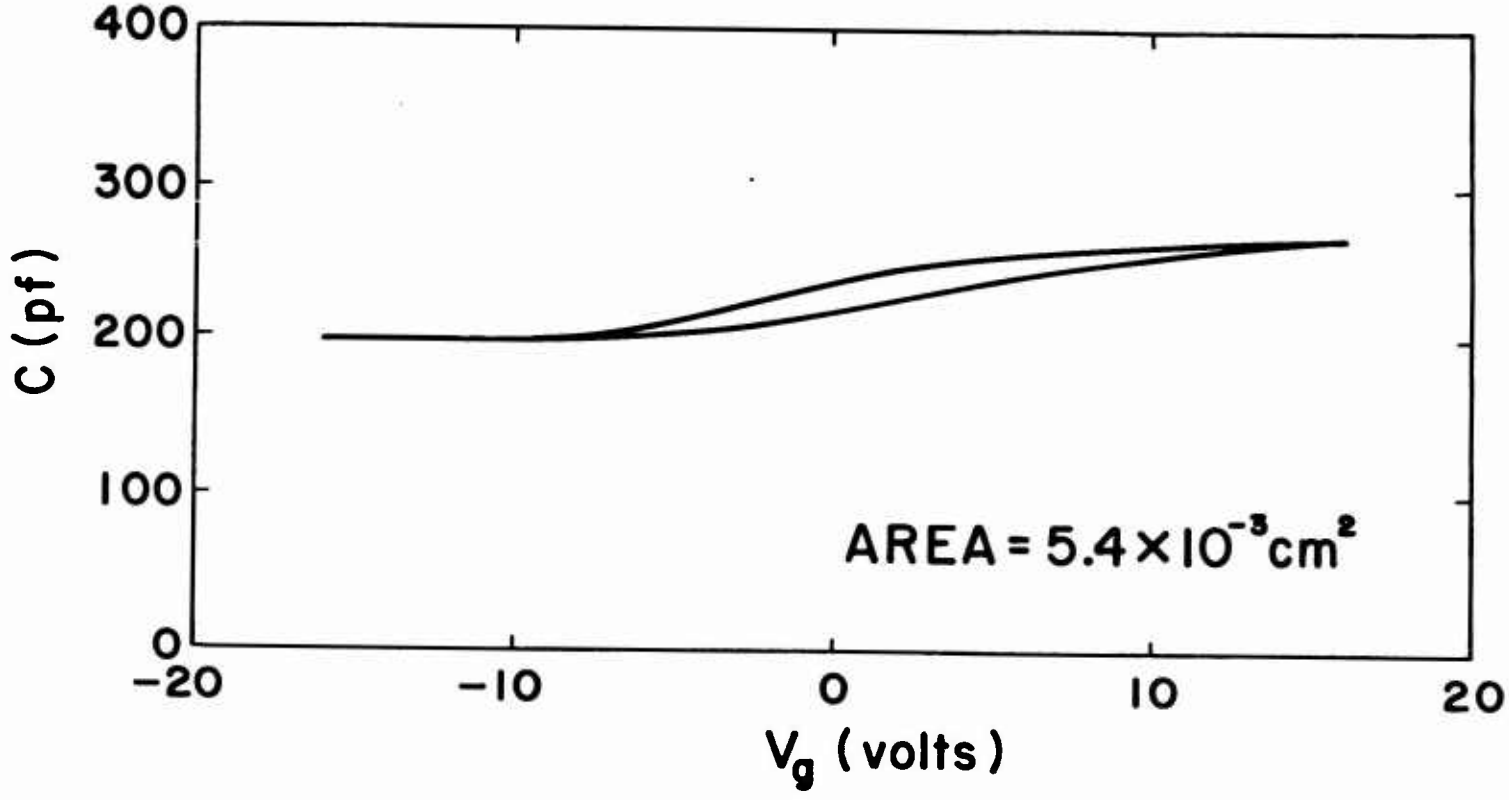


FIG. 4

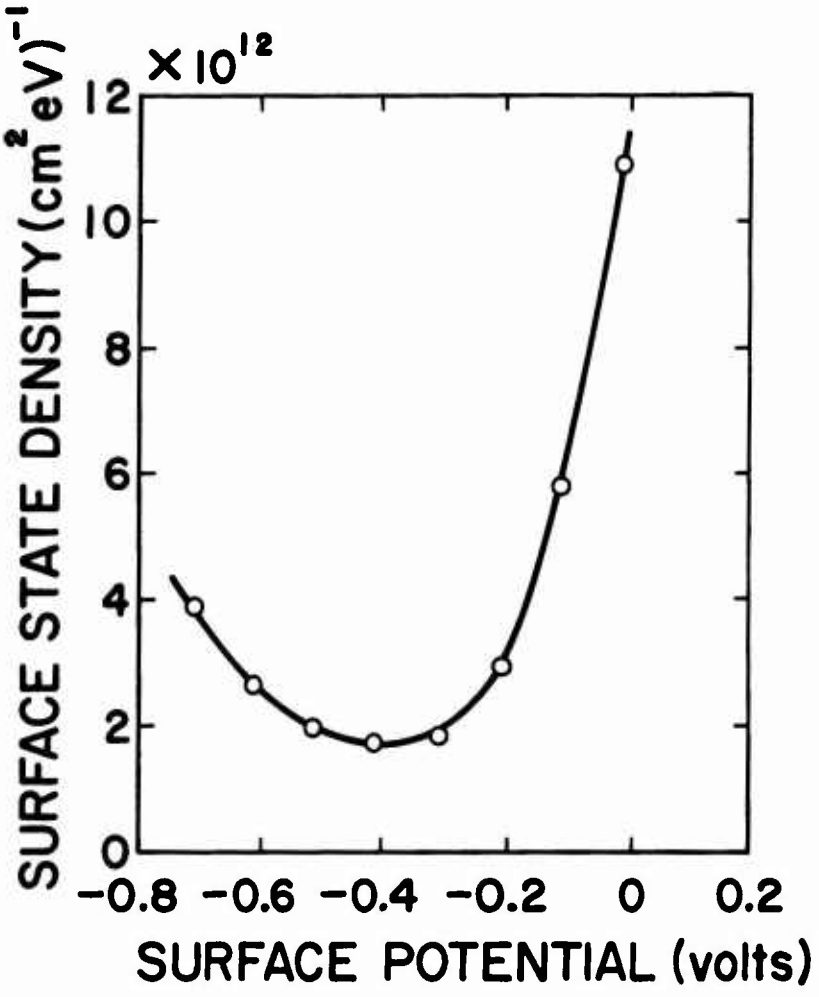

SURFACE STATE DENSITY (cm² eV)⁻¹
X 10¹²
12
10
8
6
4
2
0
-0.8
-0.6
-0.4
-0.2
0
0.2
SURFACE POTENTIAL (volts)

FIG.5